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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/085,307 | 02/27/2002 | James P. Kardach | 42390P13471 | 7540 |

7590 11/04/2004

David N. Tran
Blakely, Sokoloff, Taylor & Zafman LLP
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025-1030

| EXAMINER | |
|---|---|
| SURYAWANSHI, SURESH | |
| **ART UNIT** | **PAPER NUMBER** |
| 2115 | |

DATE MAILED: 11/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/085,307 | KARDACH, JAMES P. | |
| | Examiner | Art Unit | |
| | Suresh K Suryawanshi | 2115 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *27 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) *16-33* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☒ Claim(s) *1,5,6 and 10* is/are objected to.

8)☒ Claim(s) *16-33* are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/26/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Election/Restrictions*

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-15, drawn to a processor power control using non-cacheable bus master memory, classified in class 713, subclass 320 and class 711, subclass 138.

II. Claims 16-33, drawn to a processor power control using write-through cacheable bus master memory, classified in class 713, subclass 320 and class 711, subclass 142.

2. The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention I has separate utility such as using non-cacheable bus master memory without the need of write-through cacheable bus master memory. See MPEP § 806.05(d).

3. Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

4. During a telephone conversation with Edwin Taylor (Reg. No. 25,129) on Oct. 18, 2004, a provisional election was made without traverse to prosecute the invention of Group I, claims 1-15. Affirmation of this election must be made by applicant in replying to this Office action. Claims 16-33 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

5. Claims 1-15 are presented for examination.

### *Claim Objections*

1. Claims 1 and 6 are objected to because of the following informalities: a claim should end with a period. Appropriate correction is required.

2. Claims 5 and 10 are objected to because of the following informalities: use of abbreviation "ARB_DIS" without an establish definition in the claim itself or in the parent claim. Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

3. Claims 1 and 6 recite the limitation "the processor" in the last line. There is insufficient antecedent basis for this limitation in the claim.

### *Claim Rejections - 35 USC § 103*

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Poisner et al (US Patent no 5,983,354[1]) in view of Elkhoury et al (US Patent no 6,205,507 B1).

6. As per claims 1, 6 and 11, Poisner et al clearly disclose that a necessary requirement for placing a processor into a low power state (C3 state) is to make sure that no bus master device is communicating with main memory because in C3 state the processor will be unable to maintain cache coherency with main memory [col. 1, line 66 – col. 2, line 11; col. 5, lines 6-9; col. 8, lines 25-38]. Now, a routineer in the art would think how to keep the processor in C3 state while bus master device still can use the memory for other purposes where no cache coherency is required. This can be done by setting the memory as non-cacheable which is expressly disclosed by Elkhoury et al that the snoop routine from the processor will not be executed if the memory is set as non-cacheable [col. 6, lines 23-28]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as both are directed to cache coherency between a processor and main memory accessed by a bus master device. Moreover, clearly the idea of setting the memory as non-cacheable will allow to place the processor in the computer system into a low power state of C3 because now the processor does not have to maintain it's cache coherency and the same time there will be no need of setting a bus master status bit. Thus, a bus master device will be able to utilize the main memory for other purposes.

[1] Poisner et al is a prior art reference cited by applicant dated Jan 26, 2004.

7. As per claims 2, 7 and 12, Poisner et al teach that the low power state is a deep sleep state [col. 1, lines 47-48].

8. As per claims 3, 8 and 13, Poisner et al teach that the low power state is a C3 state [col. 8, lines 36-37].

9. As per claims 4, 9 and 14, Elkhoury et al teach that there is no snoop cycles are generated when the memory is set as non-cacheable [col. 6, lines 23-28].

10. As per claims 5, 10 and 15, clearly in the view of the detailed discussion above in claim 1, the bus master device is allowed to generate bus master read and write operation even when the ARB_DIS bit is set.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suresh K Suryawanshi whose telephone number is 571-272-3668. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sks
October 26, 2004

Dennis M. Butler

**Dennis M. Butler**
**Primary Examiner**